

ABSTRACT OF THE DISCLOSURE

Memory devices are adapted for direct interface or virtual integration with a processor or other logic device through a local bus and isolated from a system bus. Such memory devices are capable of lower power requirements and reduced size due in part to the elimination of certain redundant circuitry. Direct interfacing through the local bus facilitates the elimination or reduction of input/output (I/O) buffer circuitry by eliminating the need to step up to and step down from typical system bus voltage levels.

Communication between the memory device and a separate logic device occurs across the local bus at voltage levels compatible with internal logic levels of the memory device.

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